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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAYNE, DAVID C	

ART UNIT	PAPER NUMBER
2633	7

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/784,419	CAO, JUN	
	Examiner	Art Unit	
	David C. Payne	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7, and 11-18* is/are rejected.

7)☒ Claim(s) *5,6, 8-10, 19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *#4 and #6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo US 5,619,148 (Guo) in view of Ewen et al. US 5,301,196 (Ewen).

Regarding claims 1, 3, 7, 11

Guo disclosed,

A method of recovering a clock and data from a data signal comprising: receiving the data signal having a first data rate; receiving a clock signal having a first clock frequency, and alternating between a first level and a second level (Figure 1B, Col. 4, lines 5-15); storing the data signal when the clock signal alternates from the first level to the second level (Figure 5, #510), and providing the stored data signal as a first signal a first amount of time later; storing the first signal when the clock signal alternates from the first level to the second level, and providing the stored first signal as a second signal a second amount of time later (Figure 5, #530); providing a third signal by delaying the first signal for a third amount of time (Figure 5, #561); Guo does not disclose,

storing the third signal when the clock signal alternates from the second level to the first

level, and providing the stored third signal as a fourth signal a fourth amount of time later; providing a fifth signal by delaying the data signal a fifth amount of time; providing an error signal by taking the exclusive-OR of the first signal and the fifth signal; and providing a reference signal by taking the exclusive-OR of the second signal and the fourth signal, wherein the first data rate is equal to the first clock frequency.

Ewen disclosed taking the exclusive-OR (Figure 1 #104) of the first signal and another signal where the first data rate is equal to the first clock frequency. It would have been obvious to one of ordinary skill in the art at the time of invention to form a signal indicating whether the generated clock leads or lags the received data as taught by Ewen (see Col. 2, lines 25-35). This signal is fed back to the ring oscillator to adjust the phase of the clock relative to the phase of the received data. While Guo and Ewen do not disclose the third and fourth signal storage, it would have been obvious to one of ordinary skill in the art at the time of invention to include further storage elements to further delay the signals provide a more granular time delay recovery apparatus by having delay for each storage element.

Regarding claim 2, Ewen disclosed

applying the error signal (Figure 1 #112) and the reference signal to a loop filter (Figure 1 #113) to generate a loop filter output.

Regarding claims 3 and 4, Ewen disclosed

wherein the providing the error signal and providing the reference signal is done by exclusive-OR gates. (Figure 1 #104)

3. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo US 5,619,148 (Guo) in view of Ewen et al. US 5,301,196 (Ewen) as applied to claim 11 above, and in further view of Homol et al. US 6,570,946 B1 (Homol).

   Regarding claims 12 and 13, the modified invention of Guo and Ewen do not disclose using differential signals at the data input and clock inputs to the flip-flops. Homol disclosed differential input (Figure 8 #206). It would have been obvious to one of ordinary skill in the art at the time of invention to use differential inputs in the modified invention to provide immunity to noise and fast switching as disclosed by Homol see Col. 5, lines 8-20.

   Regarding claim 14, Ewen disclosed

   wherein the providing the error signal and providing the reference signal is done by exclusive-OR gates. (Figure 1 #104)

4. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo US 5,619,148 (Guo) in view of Ewen et al. US 5,301,196 (Ewen) as applied to claim 11 above, and in further view of Rokugawa US 5,923,455 (Rokugawa).

   Regarding claims 15 and 16,

   the modified invention of Guo and Ewen does not disclose the embodiment of the clock recovery circuit in a optical receiver and transmitter. Rokugawa disclosed a similar clock recover circuit used in optical transmission (Figure 4). It would have been obvious to one of

ordinary skill in the art at the time of invention to use the modified invention in a optical receiver/transmission circuit for the benefit of identifying data in phase relationship to a clock signal as disclosed by Rokugawa, (see co. 3, lines 60-65).

Regarding claim 17,

the modified invention of Guo and Ewen a photo-diode (Col. 5, lines 55-65, Figure 4 #44), configured to receive optical signals; a receive amplifier (#45) coupled to the photo-diode; the modified invention of Guo and Ewen does not disclose

a light emitting diode, configured to transmit optical signals; a transmitter coupled to the light emitting diode and a media access controller. However, it would have been obvious to one of ordinary skill in the art at the time of invention to include an LED or media access controller as these are well known components in optical systems and would be need to complete two way transmission between nodes.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guo US 5,619,148 (Guo).

Regarding claims 18

Guo disclosed,

A method of modifying a signal path comprising an output of a first flip-flop level (Figure 5, #510) coupled to an input of a second flip-flop level (Figure 5, #510) and the output of the first flip-flop and an output of the second flip-flop coupled to a logic gate level (Figure 5,

#531), the flip-flops clocked on consecutive transitions of a clock signal, the method comprising:

Guo disclosed a delay element (Figure 5 #533, Col. 10, lines 1-15) between the second and Guo does not disclose, inserting a delay element between the output of the first flip-flop and the input of the second flip-flop, wherein a delay through the delay element is greater than a duration between consecutive transitions of the clock signal, less a clock-to-Q delay for the first flip-flop, and plus a hold time for the second flip-flop; and inserting a third flip-flop between the first flip-flop and the logic gate, an input of the third flip flop coupled to the output of the first flip-flop, and an output of the third flip-flop coupled to the logic gate. While Guo does not disclose the third and fourth signal storage, it would have been obvious to one of ordinary skill in the art at the time of invention to include further storage elements to further delay the signals provide a more granular time delay recovery apparatus by having delay for each storage element.

Allowable Subject Matter

6. Claims 5,6, 8-10, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David C. Payne whose telephone number is (703) 306-0004. The examiner can normally be reached on M-F, 7a-4p.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dcp

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